LOW POWER IF／AF PLL CIRCUIT FOR NARROW BAND FM RECEIVER

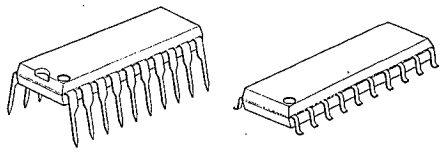
■ GENERAL DESCRIPTION

The NJM2206 is a low power IF/AF PLL circuit for narrowband FM receiver with single or double balanced mixer-IF amplifier and detector. Its low power characteristic is capable for battery operation and remote control.

This device is capable of high signal to noise ratio by PLL detector and high channel separation ratio performance.

Since the NJM2206 can operate 1st IF input frequency at 25MHz and 2nd IF input frequency at 800kHz, the IC is suited for CB transceiver, wireless control system, and other communication systems.

■ PACKAGE OUTLINE

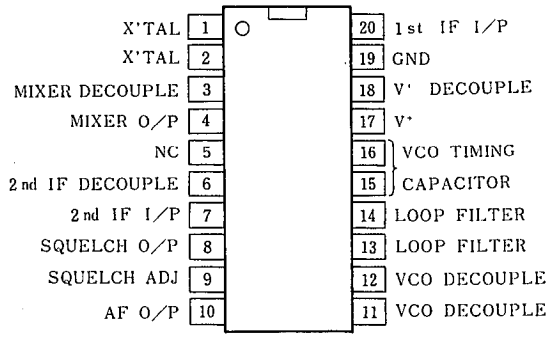


NJM2206D　　NJM2206M

■ FEATURES

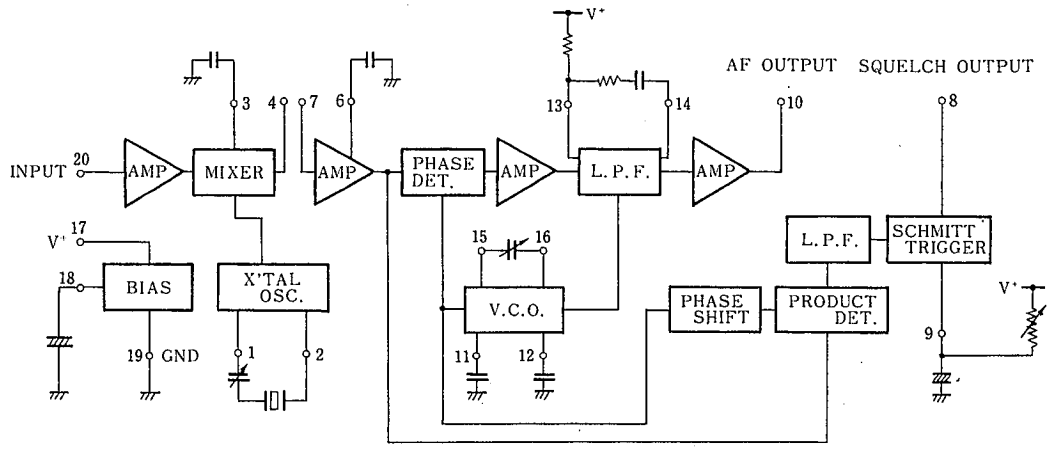
- High Sensitivity
- Low Operating Current　　2.8mA(V^+=7V)
- High S/N Ratio　　47dB(Typ)
- Less Number of External Components
- Package Outline　　DIP20, DMP20
- Bipolar Technology

■ PIN CONFIGURATION



NJM2206D
NJM2206M

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Power Dissipation	P_D	(DIP20) 700	mW
		(DMP20) 350	mW
Operating Temperature Range	T_{opr}	−20~75	℃
Storage Temperature Range	T_{stg}	−40~125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=7V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}		—	2.8	3.8	mA
1st IF Frequency Bandwidth	f_{B1}		—	25	—	MHz
1st IF Amp. Gain	G_{V1}		—	20	—	dB
Mixer Conversion Gain	g_{VM}		—	15	—	dB
2nd IF Amp. Gain	G_{VM}		—	60	—	dB
Input Singal Dynamic Range	V_{IDR}	for AF Output 1dB deviation	—	100	—	dB
Maximum Input Level	V_{IMAX}		0.2	—	—	Vrms
Input Sensitivity	S/N 1	At Input Level 10μVrms	20	—	—	dB
Signal to Noise Ratio	S/N 2	Input Level 1mVrms	40	45	—	dB
Total Harmonic Distortion	THD	Input Level 1mVrms	—	—	3	%
AF Output Level	V_O	Input Level 1mVrms	24	30	36	mVrms
AM Suppression Ratio	SUP_{AM}	for 30% AM at Input Level 100μVrms	—	30	—	dB
Squelch Low Level	V_{SL}	10μVrms Input	—	0.1	1.0	V
Squelch High Level	V_{SH}	0.5μVrms	5.0	6.4	—	V

The test conditions are as designated below, unless otherwise specified.

1st IF: 20.8MHz, 2nd IF: 455kHz, Modulation frequency: 1kHz

Frequency deviation: 3.5kHz

Test circuit diagram: See attached figure.

Ideal jigs shall be used.

■ DESCRIPTION OF OPERATION

[1] IF AMP, MIXER, and LOCAL OSC

(1) 1st IF Amp

Pin (20) is the signal input terminal. The 1st IF amplifier has the frequency characteristic shown in Graph 1 and the I/O characteristic shown in Graph 2. Also, Graph 3 shows the input impedance-to-frequency characteristic, while Graph 4 shows the input level-to S/N characteristic.

(2) Local OSC

This local OSC is composed by connecting a crystal oscillator and series capacitor across pins (1) and (2). The series capacitor is connected for finely adjusting the oscillation frequency and reducing the temperature drift.

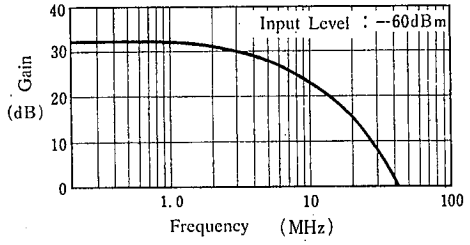
Graph 5 shows the oscillation frequency-to-power voltage and the oscillation level-to-power characteristic.

Graph 6 also shows a change of the oscillation frequency to the capacitance of the capacitor connected in series. For details, please contact the crystal oscillator maker.

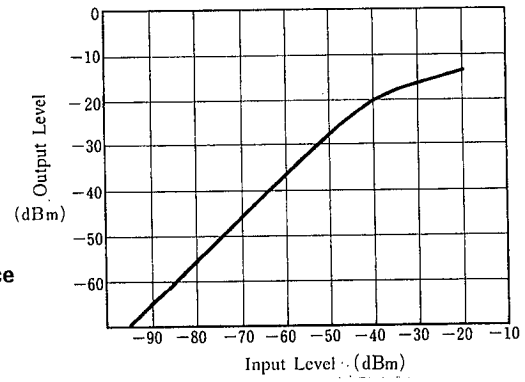
(3) Mixer

The mixer circuit produces the 2nd IF frequency by mixing the 1st IF Amp output and local OSC output signal with each other. A decoupling capacitor is connected to pin (3).

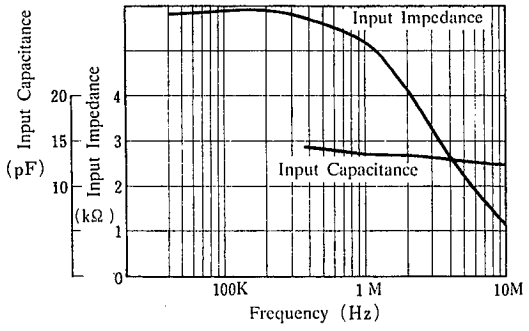
Graph-1 1st IF Amp Frequency Response



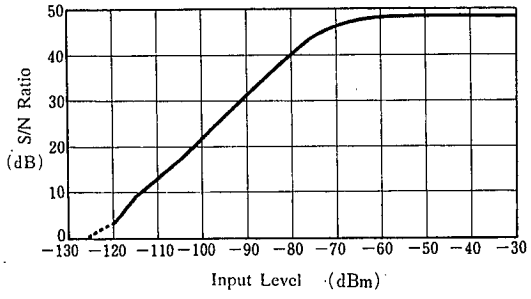
Graph-2 1st IF Amp Input-output Character



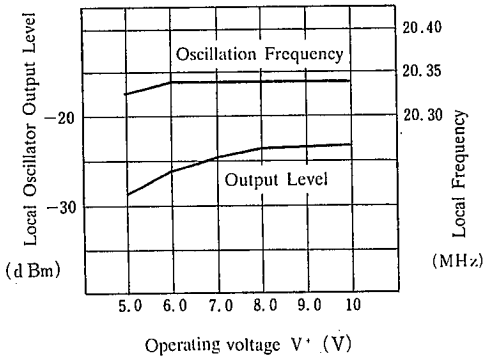
Graph-3 Input Impecance/Capacitance vs. Frequency



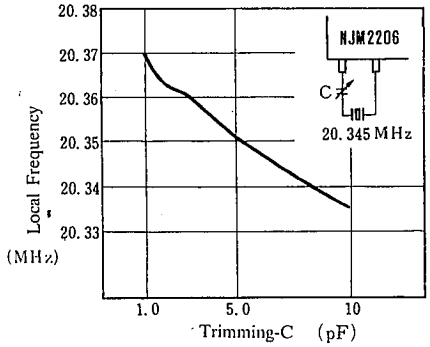
Graph-4 Input Level vs. S/N Ratio



Graph-5 Local Oscillator Output Level/Freq. vs. Operating Voltage



Graph-6 Trimming-C vs. Local Frequency



Note) It is depending on the crystal oscillator.

(4) Pin (4)–GND Capacitor

The capacitor to be connected across pin (4) and GND composes a low-pass filter as shown in Fig. 1.

The cutoff frequency $f_c = 1/2\pi CR$

This cutoff frequency f_c is set to be more than two times the 2nd IF frequency. This C is about 80pF maximum, and it can suppress higher harmonics components without affecting the 455kHz output.

This behaviour is shown in Graph 7.

(5) The capacitor across pins (4) and (7) serves as the coupling capacitor for the mix out and 2nd IF Amp stage. A ceramic filter is insertable instead of the coupling capacitor.

(6) The S/N ratio is changed by the capacitor across pin (6) and GND when the input level is low as shown in Graph 8. this is because the capacitor across pin (6) and GND serves as the decoupling capacitor in the 2nd IF Amp stage, so that the 2nd IF Amp gain is reduced when this capacitance of the capacitor decreases.

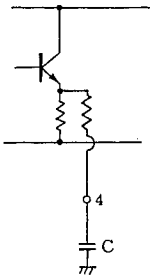
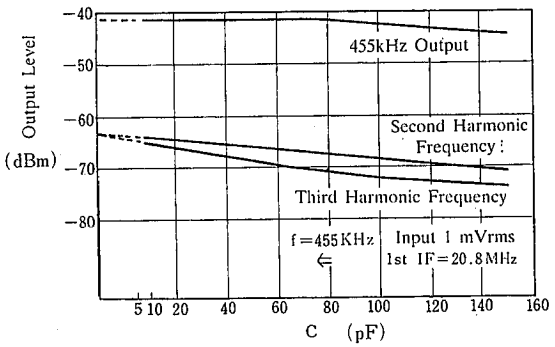
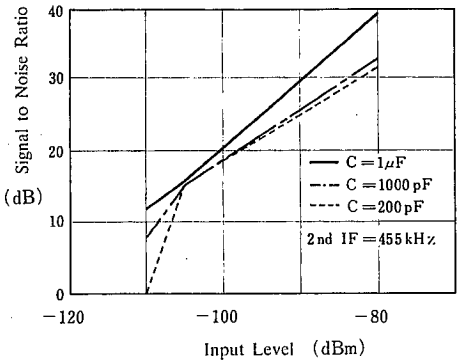


Fig. 1

Graph-7 Pin (4) Low-pass Filter C Value-higher Harmonics component



Graph-8 Change of Input Sensitivity by Pin (6) Decoupling Capacitor



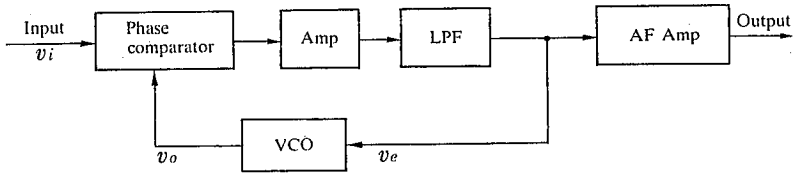
[2] Operation Principle of PLL Demodulation

(1) Operation principle of NJM2206 FM demodulator circuit

When FM is locked at the center frequency, the oscillation frequency of VCO follows frequency change of the FM input VCO oscillation frequency to the input signal frequency and, the control voltage becomes the demodulated output. VCO oscillation frequency to the input signal frequency and, the control voltage becomes the demodulated output.

The FM demodulation circuit of NJM2206 is constructed as shown in BLOCK DIAGRAM 2.

Fig. 2 PLL Demodulation Circuit Block Diagram



Assume v_i be the input signal voltage and v_o be the VCO signal voltage in Fig. 2.

$$v_i = V_i \sin \{\omega_i t + \theta_i(t)\} \quad \cdots\cdots (1)$$

$$v_o = V_o \cos \{\omega_o t + \theta_o(t)\} \quad \cdots\cdots (2)$$

From equations (1) and (2), signal voltage v_e after eliminating high-frequency components via the LPF is obtained by equation (3).

$$v_e = K_D \cdot F(S) \cdot \sin \{(\omega_i - \omega_o)t + \theta_i(t) - \theta_o(t)\} \quad \cdots\cdots (3)$$

Where F(S): Transfer function of LPF

K_D: Conversion gain of phase comparator

When the angular frequency of the input signal coincides with the angular frequency of the output signal, error voltage n_e proportional to the phase differences is obtained as shown in equation (4).

$$\nu_e = K_D \cdot F(S) \cdot \sin \{ \theta_i(t) - \theta_o(t) \}$$
$$\approx K_D \cdot F(S) \{ \theta_i(t) - \theta_o(t) \} \quad \cdots\cdots (4)$$

Also, the ν_e-to-VCO angular frequency ω_o relation is represented by equation (5).

$$\omega_o = \omega_f + K_o \nu_e \quad \cdots\cdots (5)$$

where ω_f: Free-running angular frequency of VCO

K_o: Conversion gain of VCO

Since the microscopic change of the phase angle with time is given by the angular frequency change component $\Delta\omega_o$ we obtain; $\Delta\omega_o = K_o \cdot \nu_e = d\theta_o(t)/dt$ ..... (6)

From equations (5) and (6), we obtain the PLL transfer function as shown in equation (7)

$$H(S) = \frac{\theta_o(S)}{\theta_i(S)} = \frac{KF(S)}{S+KF(S)} \quad \cdots\cdots (7)$$

where $K = K_o \cdot K_D$: Loop gain coefficient

Assume that $\theta_e(S) = \theta_i(S) - \theta_o(S)$, and we obtain equation (8) from equation (7);

$$\frac{\theta_e(S)}{\theta_i(S)} = \frac{S}{S+KF(S)} \quad \cdots\cdots (8)$$

Let's consider about the phase difference of the input signal and VCO output signal when the angular frequency of the input signal has changed stepwise by $\Delta\omega$, while PLL is being locked.

Since $\theta_i(S) = \Delta\omega/S^2$, we obtain from equation (8)

$$\lim_{t\to\infty} \theta_e(t) = \lim_{S\to 0} \theta_e(S) = \frac{\Delta\omega}{KF(S)} \quad \cdots\cdots (9)$$

It is understood from equation (9) that phase difference θ_e between the input signal and VCO output signal is proportional to angular frequency deviation $\Delta\omega$ values.

From equation (9), $\theta_e = \Delta\omega/KF(S)$. Error voltage ν_e produced when the phase difference θ_e has been generated is obtained from equation (4) as follows;

$$\nu_e = K_D \cdot F(S) \cdot \theta_e \quad \cdots\cdots (10)$$

From equation (10),

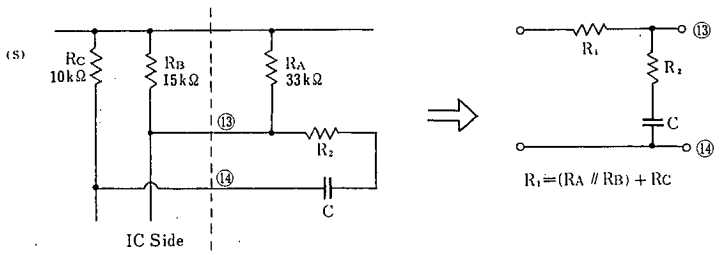
$$\nu_e = \Delta\omega/K_o \quad \cdots\cdots (11)$$

The output voltage of the phase comparator (after the LPF stage) is proportional to the angular frequency deviation of the input signal when a phase difference has been produced. Accordingly, this error voltage serves as the demodulated output of the FM signal as it is.

References: "Phase lock techniques" Floyed M Gardner
"Basis and application of PLL", Hideo Kadota

(2) Low-pass filter (LPF)

The LPF of NJM2206 is shown in Fig. 3.



Transfer Function $F(S) = \dfrac{S\tau_2 + 1}{S(\tau_1 + \tau_2) + 1}$ $\quad \tau_1 = CR_1, \quad \tau_2 = CR_2$

Fig. 3 NJM2206 LPF

The loop band is determined by this LPF, and it affects the maximum phase deviation capture range, maximum frequency response characteristic, or noise bandwidth. The PLL transfer function is obtained when the LPF shown in Fig. 2 is used.

$$H(S) = \frac{S\omega_n(2\xi - \frac{\omega_n}{K}) + \omega_n}{S^2 + 2\xi\omega_n S + \omega_n}$$

$\omega_n = \left(\frac{K}{\tau_1 + \tau_2}\right)^{1/2}$: Natural angular frequency

$\xi = \frac{1}{2}\left(\frac{K}{\tau_1 + \tau_2}\right)^{1/2}\left(\tau_2 + \frac{1}{K}\right)$: Dumping factor

When $K \gg 1$, $\xi = \frac{1}{2}\omega_n \tau_2$

This filter is characterized that since the loop gain, and damping factor are adjustable separately, the narrow band is obtainable with high stability of PLL.

Exmaple of calculation of LPF constants

$K_o = 0.5f_o$: Conversion gain of VCO, f_o: free-running frequency

$K_D = 1.96$: Conversion gain of phase comparator x gain of amplifier

$K_oK_D = 0.98f_o$

$R_1 = 20k\Omega$

The above values are calculated from the design values of the NJM2206 circuit constants.

Assume that the maximum frequency deviation $\Delta f = 3.5kHz$, the modulation signal frequency $f_m = 1kHz$, $f_o = 455kHz$ and the maximum phase error $\phi_{e\,max}$ is obtained by;

$$\phi_{e\,max} = \frac{2\pi}{K_oK_D} \cdot \frac{\Delta f}{f_o} = 0.05$$

Assume that natural angular frequency $f_n = 10kHz$, and we obtain from Fig. 3;

$$\frac{\phi_e}{\frac{\Delta f}{f_n}} = 0.1$$

$$\phi_e = 0.1 \times \frac{\Delta f}{f_n} = 0.035$$

Accordingly, we obtain, assuming that $f_n = 10kHz$;

$$\tau_1 + \tau_2 = \frac{K_oK_Dfo}{(2\pi fn)^2} = 113\mu S$$

Damping factor $\xi = 0.707$,

$$\tau_2 = \frac{2\xi}{2\pi fn} = 22\mu S$$

$$\therefore \tau_1 = 91\mu S$$

From these values, we obtain C and R_2 as follows.

$C = \tau_1/R_1 = 4500pF$

$R_2 = \tau_2/C = 4.9k\Omega$

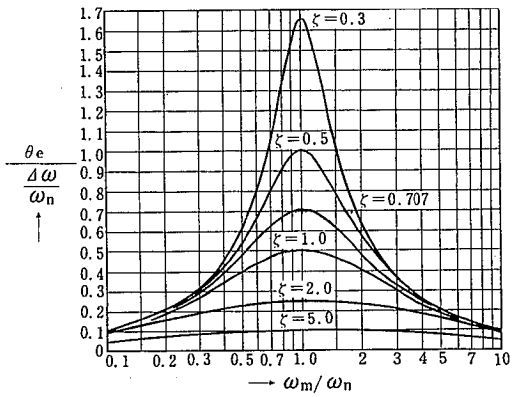


Fig. 4 Steady-state Phase Error by Sine Wave FM

(3) Effect of LPF constants on the detection characteristic of PLL demodulator circuit

Graphs 9, 10 and 11 show the input-to-output characteristic, modulation frequency-to-AF output characteristic, and frequency deviation-to-distortion factor characteristic when LPF constants were changed, respectively. Table 1 shows LPF constants in these cases.

- **Input-to-output characteristic (Graph 9)**

The noise level from −100dBm to −70dBm is affected by the natural angular frequency and lock range. Since the input level, where the noise level suppression is started, is transient just before the PLL is locked, the noise level is affected by the damping factor and capture range.

- **Modulation frequency-to-AF output characteristic (Graph 10)**

The band is demodulated from (1) and (2), and determined by the natural angular frequency. If this band is wide, the noise level increases.

- **Frequency deviation-to-distortion factor characteristic (Graph 11)**

The maximum frequency deviation is determined by the natural angular frequency.

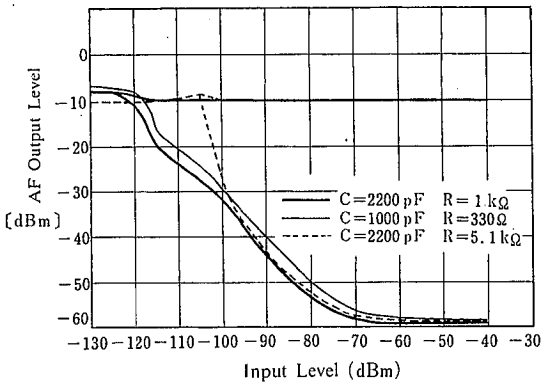
- **LPF constants, the capture range, and lock range (Graph 12)**

Graph 12 shows the capture range and lock range when LPF constants were changed. From this graph and the input-to-output characteristic shown in Graph 9, it is understood that the noise level is changed by the lock range.

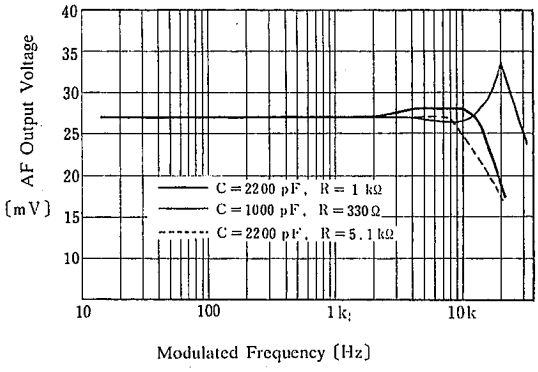
Table-1

①	C=2200pF, R_2 =1kΩ	f_n =15.6kHz, ξ=0.1
②	C=1000pF, R_2 =330Ω	f_n =23.6kHz, ξ=0.02
③	C=2200pF, R_2 =5.1kΩ	f_n = 14.3kHz, ξ=0.5

Graph 9 Input-output Characteristic



Graph 10 Modulated Frequency vs. A.F. Output Voltage



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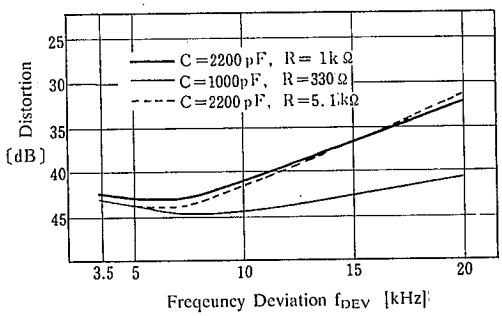
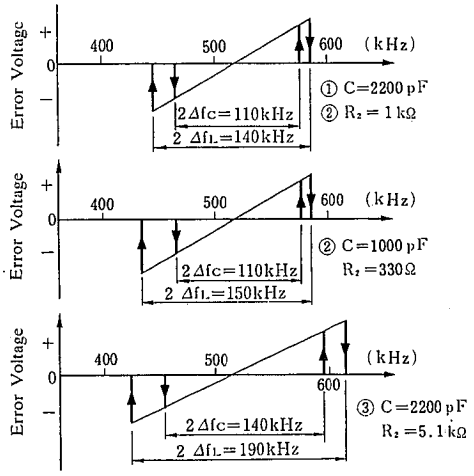
Graph 11 Frequency Deviation vs. Distortion



Graph 12 LPF Constance, Capture Range, Lock Range



Δf_C: Capture Range Δf_L: Lock Range

(5) VCO

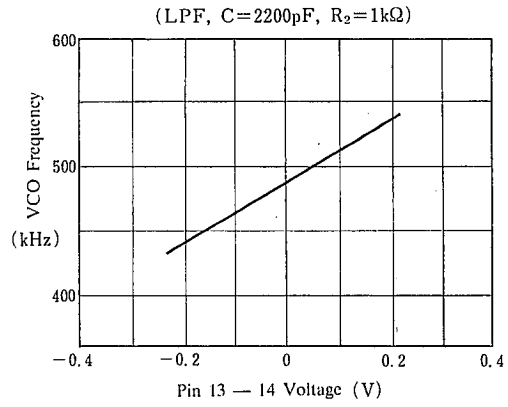
Graph 13 shows the VCO oscillation frequency-to-LPF output voltage characteristic. The LPF output voltage (voltage across pins (13) — (14)) becomes the VCO control voltage.

As shown in Graph 13, this relation is linear, and its gradient is determined by the VCO converstion gain.

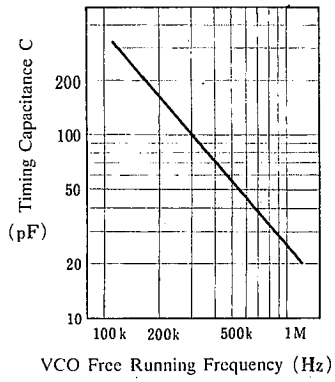
Also, the linearity range is closely related to the lock range. Graph 14 shows the VCO free-running-to-timing C characteristic to show a change of the VCO free-running frequency when timing C is changed.

The capacitor connected across pins (11), (12) and GND suppresses the higher harmonics of the VCO output.

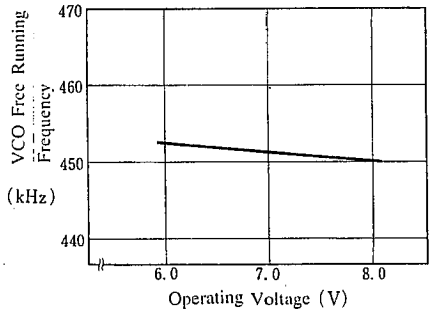
Graph 13 VCO Frequency vs. LPF Output Voltage



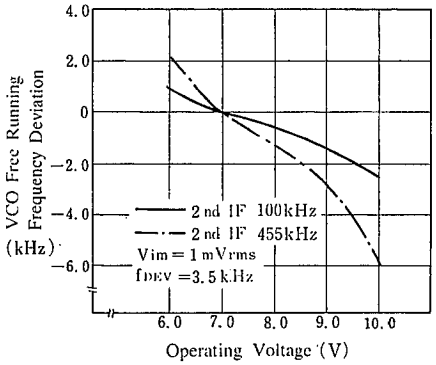
Graph 14 VCO Free Running Frequency vs. Timing Capacitance



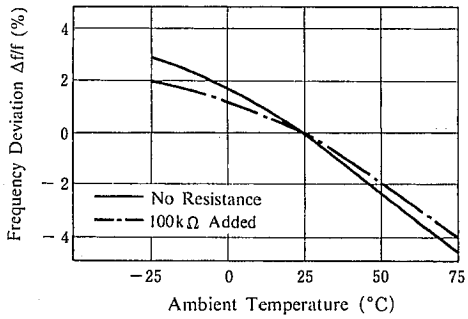
Graph 15 VCO Free Running Frequency vs. Operating Voltage



Graph 16 VCO Free Running Frequency Deviation vs. Operating Voltage

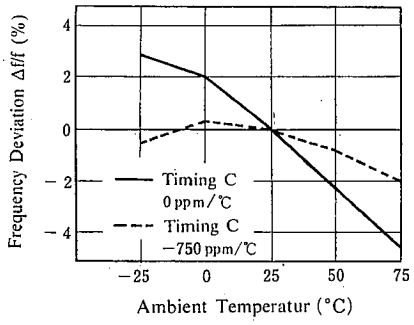


Graph 17 VCO Frequency Deviation vs. Ambient Temperature



Connection Resistance between pin 1 and 12
Use timing Capacitance at 0 ppm/°C

Graph 18 VCO Frequency Deviation vs. Ambient Temperature



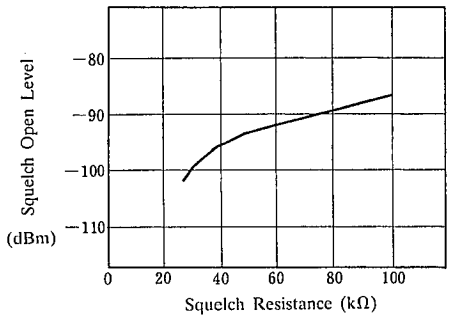
[3] Squelch Circuit Function

The squelch sensitivity is adjustable by the resistance value R connected between pin (9) and V^+. Graph 19 shows the relation between resistance R and squelch release level. As shown in graph 20, the squelch sensitivity corresponding to the S/N ratio required for mute function is adjustable by resistance R. Graph 21 shows the power voltage-to-squelch release level characteristic. Also, the squelch attack time is adjustable by the capacitor connected across pin (9) and GND. This characteristic is obtained by changing the gradient of the squelch level from a high level to a low level by using an external capacitor.

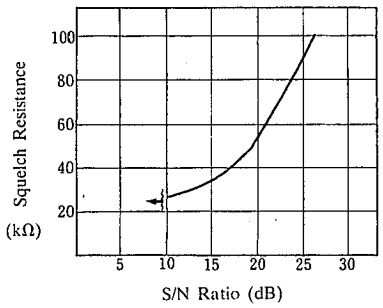
(Note) Squelch release level: Input signal level when the squelch level (pin (8) DC potential) changes from the high level to low level.

The VCO timing C is adjustable by maximizing the DC voltage of pin (9) when an 1mVrms non-modulated signal input is applied.

Graph 19 Squelch Open Level vs. Squelch Resistance

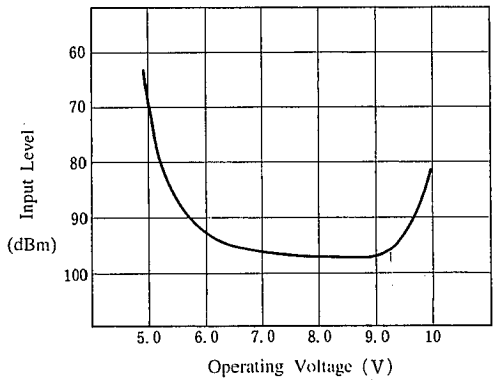


Graph 20 Squelch Sensitivity Characteristics

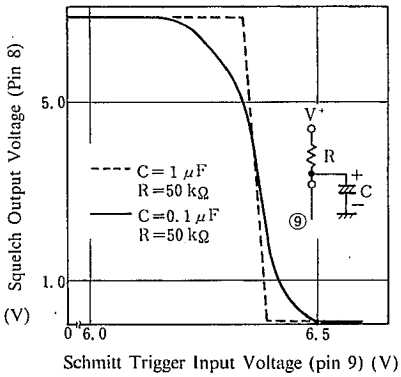


Graph 21 Squelch Open Level vs. Operating Voltage

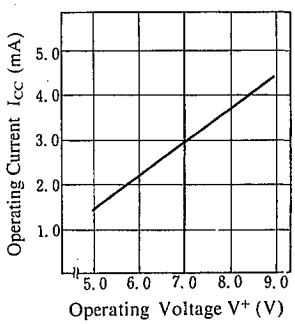
(C=1.0μF, R=5.0kΩ)



Graph 22 Squelch Input/Output Characteristics



Graph 23 Operating Current vs. Operating Voltage



[4] NJM2206 overall characteristics

(1) DC characteristic

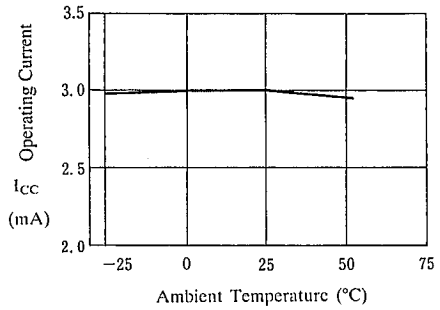
Graph 23 shows the power voltage-to-current consumption characteristic, while graph 24 shows the ambient temperature-to-current consumption characteristic.

(2) AC characteristic

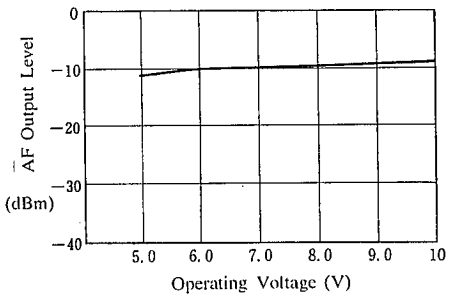
Graph 25 shows the power voltage-to-output level characteristic. As shown from this graph, this IC is characterized with small change of the AF output level against power fluctuations.

Also, the input/output characteristic is shown in graph 26. Graph 28 and 29 show the S/N ratio, sense, and AF output level-to-power voltage characteristic and the S/N ratio, sense, and AF output level-to-ambient temperature characteristic, respectively.

Graph 24 Operating Current vs. Ambient Temperature

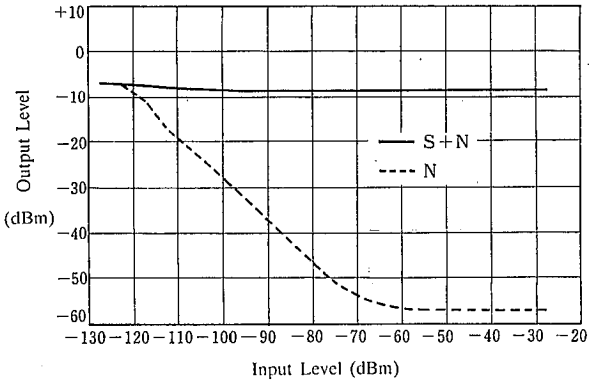


Graph 25 AF Output Level vs. Operating Voltage



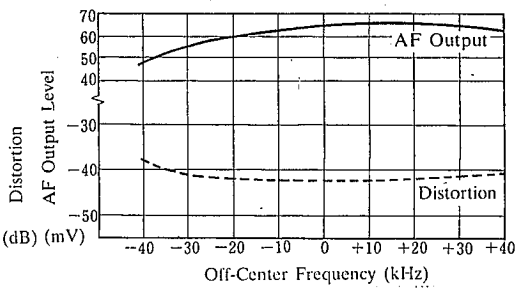
Graph 26 Input/Output Characteristics

(V^+=7.0V, f=20.8MHz, LPF, C=200pF, R=1kΩ, VCO Timing, C=60pF)



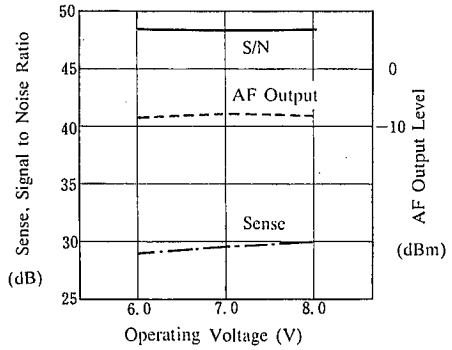
Graph 27 Distortion, AF Output Level vs. Off-Center Frequency

(V^+=7.0V, f_{DEV}=3.5kHz, V_{in}=1mVrms)



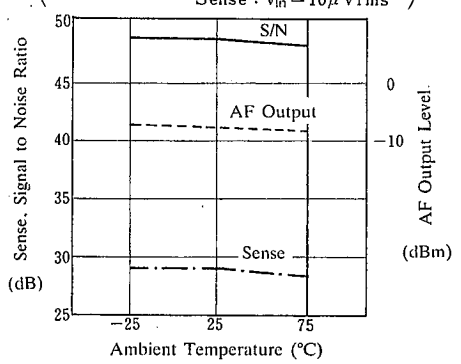
Graph 28 Signal to Noise Ratio, Sense, AF Output Level vs. Operating Voltage

(Test Condition : S/N Ratio, AF Output : v_{in}=1mVrms
Sense : v_{in}=10μVrms)

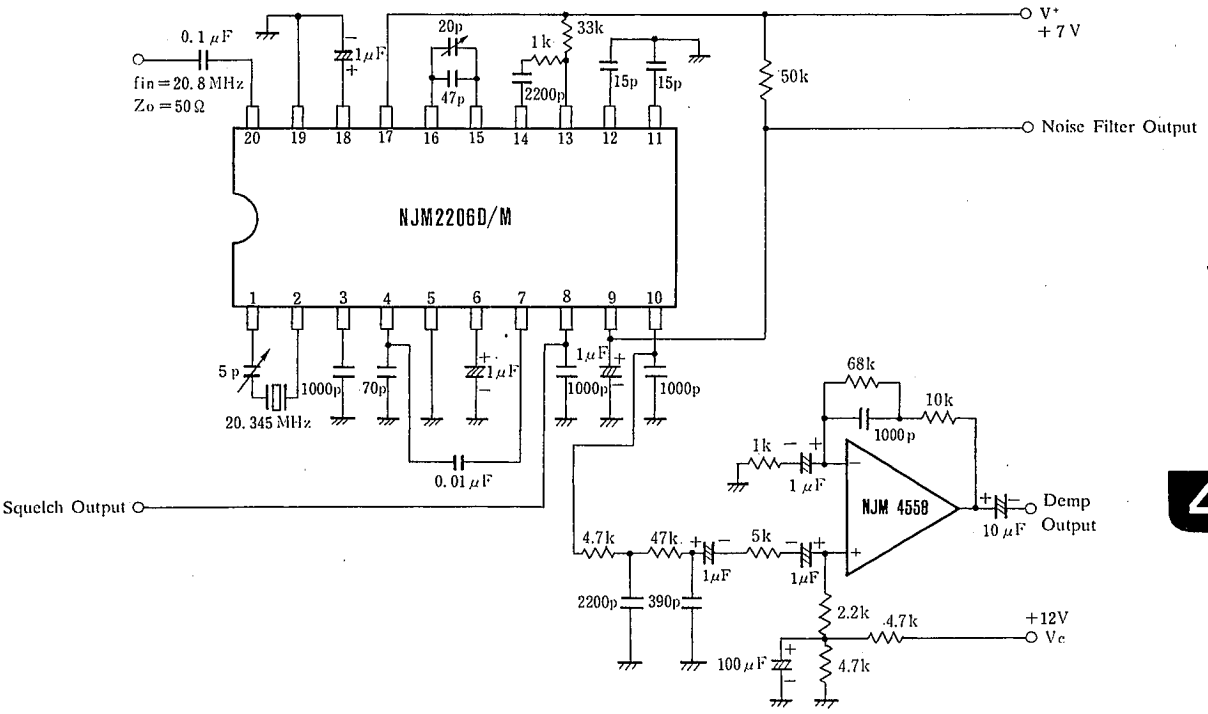


Graph 29 Signal to Noise Ratio, Sense, AF Output Level vs. Ambient Temperature

(Test Condition : S/N Ratio, AF Output : v_{in}=1mVrms
Sense : v_{in}=10μVrms)



■ TEST CIRCUIT



MEMO